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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for nonprovisional applications under 37 CFR § 1.53(b))

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First Inventor or Application Identifier	Joseph M. Brand
Title	METHOD AND APPARATUS FOR REMOVING ENCAPSULATING MATERIAL FROM A PACKAGED MICROELECTRONIC DEVICE
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. [X] Authorization for Extensions & Fee Transmittal *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages] 24 *(preferred arrangement set forth below)*
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets] 4
4. Oath or Declaration [Total Pages] 1
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)

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5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
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ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [X] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
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12. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
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[ ] Claims the benefit of Provisional Application No. _____

17. CORRESPONDENCE ADDRESS

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Respectfully submitted,

TYPED or PRINTED NAME JOHN M. WECHKIN REGISTRATION NO. 42,216

SIGNATURE _____ Date Aug. 16, 2000

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METHOD AND APPARATUS FOR REMOVING ENCAPSULATING MATERIAL FROM A PACKAGED MICROELECTRONIC DEVICE

TECHNICAL FIELD

The present invention relates to microelectronic device packages and methods and apparatuses for removing encapsulating material from microelectronic device packages.

BACKGROUND

Packaged microelectronic assemblies, such as memory chips and microprocessor chips, typically include a microelectronic die mounted to a substrate and encased in a plastic protective covering. The die includes functional features, such as memory cells, processor circuits, and interconnecting circuitry. The die also typically includes bond pads electrically coupled to the functional features. The bond pads are coupled to pins or other types of terminals that extend outside of the protective covering for connecting the microelectronic die to buses, circuits and/or other microelectronic assemblies.

In one conventional arrangement shown in Figure 1A, a die 20 is mounted to a printed circuit board (PCB) 30 with an adhesive layer 23. The die 20 has internal functional features (not shown in Figure 1A) coupled to die bond pads 33a on an external surface of the die 20. Each die bond pad 33a is connected with a wire bond 34 to a corresponding PCB bond pad 33b on a surface of the PCB 30 facing away from the die 20. Accordingly, the PCB 30 has a central aperture 31 that receives the wire bonds 34 and is aligned with the die bond pads 33a. The PCB bond pads 33b are connected to solder ball pads 32 with circuitry (not shown) internal to the PCB 30 for coupling the die 20 to other devices or circuit elements.

To encapsulate the die 20, the die 20 and the PCB 30 are positioned in a mold apparatus 40 by clamping a portion of the PCB 30 between an upper mold portion 41 and a lower mold portion 42. The die 20 is aligned with an upper cavity 43 in the upper mold portion 41 and the wire bonds 34 are aligned with a lower cavity 44 in the lower mold portion 42. A mold compound 60, such as an epoxy mold compound, is injected into the

mold cavities 43 and 44, and the encapsulated die 20 and PCB 30 are then removed from the mold apparatus 40. The periphery of the PCB 30 is trimmed to form the device package 50 shown in Figure 1B. Solder balls 35 are attached to the solder ball pads 32 for coupling the device package 50 to other devices, such as another PCB 30a having bond pads 33c aligned with the solder balls 35.

One drawback with the approach described above with reference to Figures 1A-1B for packaging the die 20 is that the mold apparatus 40 can allow the mold compound 60 to adhere to the solder ball pads 32 during the encapsulation process. For example, unclamped regions 45 of the lower mold portion 42 directly adjacent to the solder ball pads 32 are not directly supported by any corresponding structure of the upper mold portion 41 when the mold portions 41 and 42 are clamped together (by contrast, adjacent clamped regions 46a of the lower mold portion 42 are subjected to a direct normal force by corresponding clamped regions 46b of the upper mold portion 41). Accordingly, the PCB 30 can flex away from the unclamped region 45 and can allow the mold compound 60 to cover the solder ball pads 32. The mold compound 60 on the solder ball pads 32 can prevent the solder balls 35 from properly adhering to the solder ball pads 32, and can accordingly interfere with a secure electrical connection between the device package 50 and other devices or circuit elements to which the package 50 is attached. Furthermore, the flexing PCB 30 can place stresses on the die 20 that can potentially damage the die 20.

One approach to addressing the foregoing drawback is to form a trench in the lower mold portion 42 adjacent to the solder ball pads 32 for collecting any mold compound 60 that approaches the solder ball pads 32. However, such trenches are not always effective and, as the dies 20 become smaller, it can be difficult to find space between the lower cavity 44 and the solder ball pads 32 in which to position such a trench.

Another drawback with the conventional approach described above with reference to Figures 1A-1B is that it can be difficult to transfer heat away from the die 20 through the mold compound 60. Accordingly, the die 20 can overheat, which can limit the performance and/or the expected life of the die 20.

Still another drawback with the conventional arrangement described above with reference to Figures 1A-1B is that it may not be convenient to stack the device packages 50 on top of each other, a technique that can increase the number of packages 50 provided per unit area in compact electronic devices. In one conventional stacked arrangement, notches

are cut into the edges of the PCB 30 of each package 50 and a jig is used to align the notches of a first package with the notches of a second package stacked on the first package. However, this arrangement can be cumbersome and can cause damage to the dies 20, for example, if the jig is handled improperly.

SUMMARY

The present invention is directed toward methods and apparatuses for encapsulating microelectronic devices. A method in accordance with one aspect of the invention includes disposing an encapsulating material adjacent to a surface of the microelectronic substrate and exposing at least a portion of the surface of the microelectronic substrate by removing a portion of the encapsulating material adjacent to the surface. The microelectronic substrate remains in an operable condition after the portion of the encapsulating material is removed. In a further aspect of the invention, the surface of the microelectronic substrate can be exposed by directing laser radiation toward the encapsulating material to ablate the material. In other aspects of the invention, portions of the encapsulating material can be removed to form heat transfer structures in the encapsulating material and/or to expose solder ball pads of the microelectronic substrate.

The invention is also directed toward a microelectronic device package. The package can include an operable microelectronic substrate having a substrate surface and an encapsulating material at least partially covering the microelectronic substrate. The encapsulating material can have an external surface and an aperture extending through the external surface to the substrate surface, with a portion of the substrate surface exposed through the aperture. In other aspects of the invention, the encapsulating material can have an interlocking feature positioned to engage a corresponding interlocking feature of another device package to at least restrict relative movement between the device packages, for example, when the packages are stacked. In still another aspect of the invention, the device package can include heat transfer structures formed in the encapsulating material and projecting away from the substrate surface. The heat transfer structures can have at least one exposed, external heat transfer surface and can include cylindrical rods, ribs, or other shapes.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a partially schematic, cross-sectional side elevational view of an apparatus for encapsulating a die in accordance with the prior art.

Figure 1B is a partially schematic, cross-sectional side elevational view of a packaged die formed with the apparatus shown in Figure 1A.

Figure 2 is a partially schematic, cross-sectional side elevational view of an encapsulated microelectronic substrate having an exposed upper surface in accordance with an embodiment of the invention.

Figure 3A is a partially schematic, cross-sectional side elevational view of an apparatus for encapsulating a microelectronic substrate in accordance with an embodiment of the invention.

Figure 3B is a partially schematic, cross-sectional side elevational view of an encapsulated microelectronic substrate having a portion of encapsulating material removed in accordance with an embodiment of the invention.

Figure 4 is a partially schematic, cross-sectional side elevational view of two microelectronic device packages positioned for stacking in accordance with an embodiment of the invention.

Figure 5 is a partially schematic, cross-sectional side elevational view of two microelectronic device packages positioned for stacking in accordance with another embodiment of the invention.

Figure 6 is a partially schematic, top isometric view of a device package having an encapsulating material with heat transfer structures in accordance with yet another embodiment of the invention.

DETAILED DESCRIPTION

The present disclosure describes packaged microelectronic devices and methods and apparatuses for packaging such devices. Many specific details of certain embodiments of the invention are set forth in the following description and in Figures 2-6 to provide a thorough understanding of these embodiments. One skilled in the art, however, will understand that the present invention may have additional embodiments, or that the invention may be practiced without several of the details described below.

Figure 2 is a partially schematic, cross-sectional side elevational view of a device package 150 having a microelectronic substrate 120 (such as a memory die or a processor die) with an exposed upper surface 121. In one aspect of this embodiment, the microelectronic substrate 120 has a lower surface 122 facing opposite the upper surface 121. The lower surface 122 can include substrate bond pads 124 coupled to device features such as integrated circuits (not visible in Figure 2) internal to the microelectronic substrate 120. The microelectronic substrate 120 can be mounted to a support member 130 (such as a PCB) by attaching an adhesive 123 between the lower surface 122 of the microelectronic substrate 120 and an upper surface of the support member 130. In a further aspect of this embodiment, the support member 130 can have support member bond pads 133 connected to the substrate bond pads 124 with wire bonds 134. Accordingly, the support member 130 can have an aperture 131 adjacent to the support member bond pads 133 through which the wire bonds 134 pass.

In one embodiment, the support member bond pads 133 are connected to solder ball pads 132 with circuitry (not visible in Figure 2) internal to the support member 130 to form a conductive link between the support member bond pads 133 and the solder ball pads 132. Solder balls 135 can then be attached to the solder ball pads 132 for coupling the device package 150 to other electronic components, as described above. Alternatively, the device package 150 can have other conductive elements for coupling to other electronic components.

In one aspect of an embodiment shown in Figure 2, portions of the microelectronic substrate 120 and the support member 130 are surrounded by an encapsulating material 160 to protect features of the device package 150. For example, the encapsulating material 160 can include an epoxy mold compound that covers the substrate bond pads 124, the wire bonds 134, and the support member bond pads 133 after the wire bonds 134 have been connected between the microelectronic substrate 120 and the support member 130. Accordingly, the encapsulating material 160 can protect the electrical connection formed by the wire bonds 134 from corrosion and/or other environmental hazards.

In another aspect of an embodiment shown in Figure 2, at least a portion of the encapsulating material 160 is removed from the device package 150 in a region adjacent to the upper surface 121 of the microelectronic substrate 120. Accordingly, the encapsulating

material 160 can have an opening 163 aligned with the upper surface 121. In one aspect of this embodiment, the opening 163 extends through the encapsulating material 160 to the upper surface 121 to expose the upper surface 121. Alternatively, a thin layer of the encapsulating material 160 can remain adjacent to the upper surface 121 of the microelectronic substrate 120 by removing a layer of encapsulating material 160 having a thickness less than the total thickness of the encapsulating material 160 adjacent to the upper surface 121. For example, the thickness of the removed layer can be greater than 0.003 inch in one embodiment, and can have other values in other embodiments, depending on the total thickness of the encapsulating material 160. In either embodiment, a sufficient amount of the encapsulating material 160 can be removed from the region adjacent to the upper surface 121 to increase the rate at which heat can be transferred away from the upper surface 121.

In one embodiment, the opening 163 in the encapsulating material 160 is formed by positioning a laser source 170 proximate to the package 150 and directing a laser beam 171 toward the upper surface 121 of the microelectronic substrate 120. The laser beam 171 locally ablates the encapsulating material 160, forming a vapor 172 that can be convected away from the region adjacent to the device package 150. In one aspect of this embodiment, the opening 163 can be formed by repeatedly passing the laser beam 171 over the device package 150, with each successive pass removing a portion of the encapsulating material 160 until the opening 163 has the desired dimensions. Alternatively, the entire opening 163 can be formed with a single pass of the laser beam 171. In either embodiment, a single opening 163 can extend over all or a portion of the upper surface 121 of the microelectronic substrate 120. Alternatively, the opening 163 can be one of a plurality of openings, each of which extends over a portion of the upper surface 121. In another embodiment, the aperture 163 can extend over the entire upper surface of the package 150 so that the encapsulating material does not extend upwardly beyond the upper surface 121 of the microelectronic substrate 120.

In one embodiment, the power generated by the laser source 170 can be from about 4 watts to about 25 watts, and the laser beam 171 can scan over the device package 150 at a rate of from about 125 mm/sec. to about 2000 mm/sec. Adjacent scans can be about 0.025 inches wide and the laser beam 171 can be pulsed at a frequency of from about 4 kHz to about 25 kHz with a pulse width of about 8 microseconds. In other embodiments, the

laser source 170 can generate laser beams 171 having other characteristics suitable for removing the encapsulating material 160.

In still further embodiments, other techniques can be used to remove a portion of the encapsulating material 160 to form the opening 163. For example, radiation having wavelengths other than laser wavelengths can be directed toward the encapsulating material 160. Alternatively, chemical solvents, such as etchants, can be used to selectively remove portions of the encapsulating material 160 from adjacent to the substrate upper surface 121 to form the opening 163. In any of these embodiments, the techniques used to remove portions of the encapsulating material 160 are employed in a manner that does not adversely affect the operability of the microelectronic substrate 120.

One feature of an embodiment of the device package 150 described above with reference to Figure 2 is that the upper surface of the microelectronic substrate 120 is either exposed or has only a thin layer of encapsulating material 160 adjacent to it. An advantage of this feature is that heat can be more effectively and efficiently removed from the microelectronic substrate 120, for example, by convection or radiation from the substrate upper surface 121. Alternatively, a heat conductive heat sink can be attached to the exposed upper surface 121 to further increase the rate at which heat is transferred away from the microelectronic substrate 120. In either of these embodiments, the increased rate at which heat is transferred away from the microelectronic substrate 120 can enhance the performance level and/or the life expectancy of the microelectronic substrate.

Figure 3A is a partially schematic, cross-sectional side elevational view of a mold apparatus 140 for encapsulating the microelectronic substrate 120 in accordance with an embodiment of the invention. In one aspect of this embodiment, the mold apparatus 140 can include an upper mold portion 141 configured to engage an upper surface 136 of the support member 130. Accordingly, the upper mold portion 141 can have an upper cavity 143 configured to receive the microelectronic substrate 120. A lower mold portion 142 is positioned opposite the upper mold portion 141 to engage a lower surface 137 of the support member 130. The lower mold portion 142 can include a lower cavity 144 configured to receive the wire bonds 134, the support member bond pads 133 and the solder ball pads 132. Accordingly, when the encapsulating material 160 is introduced into the mold apparatus 140, it flows around the microelectronic substrate 120 and the connections between the

microelectronic substrate 120 and the support member 130 to cover the wire bonds 134, the support member bond pads 133 and at least a substantial portion of the solder ball pads 132.

In one aspect of this embodiment, the edges of the upper cavity 143 are aligned with corresponding edges of the lower cavity 144. Accordingly, the edges of the upper cavity 143 define upper contact portions 146a that are aligned with lower contact portions 146b defined by the edges of the lower cavity 144. As a result, the support member 130 is clamped uniformally from above and below. This is unlike some conventional arrangements (such as the arrangement described above with reference to Figure 1A) that have asymmetrically clamped PCBs that can allow portions of encapsulating material (flash) to penetrate between the PCB and the contact portions of the mold.

Referring now to Figure 3B, the device package 150 is removed from the mold apparatus 140 (Figure 3A) after encapsulation and a portion of the encapsulating material 160 adjacent to the solder ball pads 132 is removed to expose the solder ball pads 132 for attaching solder balls 135 (Figure 2). In one aspect of this embodiment, the laser source 170 can direct the laser beam 171 toward the encapsulating material 160 adjacent to the solder ball pads 132 to remove the encapsulating material 160 from this region. Alternatively, etchants or other chemical agents or other non-chemical agents can remove selected portions of the encapsulating material 160, so long as the surfaces of the exposed solder ball pads 132 are sufficiently clean to adhere to the solder balls 135.

In yet another alternative embodiment, an apparatus similar to that described above with reference to Figure 1A can be used to encapsulate the microelectronic substrate 120, even if the resulting package has flash extending over the solder ball pads 132. In this alternative embodiment, the laser source 170 (or another agent for removing the encapsulating material 160) can remove the flash from the solder ball pads 132. An advantage of using the mold apparatus described above with reference to Figure 1A is that existing mold apparatuses having this configuration can be used without alteration. Conversely, an advantage of the apparatus 140 described above with reference to Figure 3A is that it can support the support member 130 equally from above and below, and can accordingly reduce the likelihood for inducing stresses in the microelectronic substrate 120.

Figure 4 is a partially schematic, cross-sectional side elevational view of two device packages positioned to form a stack 290 in accordance with an embodiment of the invention. In one aspect of this embodiment, the stack 290 can include an upper package

250a stacked on a lower package 250b (referred to collectively as device packages 250). The device packages 250 are held in place relative to each other with corresponding interlocking features 251 (shown as an upper portion feature 251a and a lower portion feature 251b). For example, each package 250 can include a support member 230 (such as a PCB), a microelectronic substrate 220 attached to the support member 230, and a volume of encapsulating material 260 having an upper portion 260a above the support member 230 and a lower portion 260b below the support member 230. The upper portion 260a can have an upper portion feature 251a that interlocks with a corresponding lower portion feature 251b in the lower portion 260b to resist relative motion between the two device packages 250.

In one embodiment, the upper portion feature 251a can include a tab or projection, and the lower portion feature 251b can include a recess or cavity sized and shaped to removably receive the projection. In other embodiments, the features 251 can have other interlocking configurations. In still further embodiments, each device package 250 can have more than one feature 251 to engage the adjacent device package.

In any of the embodiments described above with reference to Figure 4, one characteristic of the interlocking features 251 is that they can be molded directly into the encapsulating material 260. Accordingly, the position of the features 251 can be consistent from one package 250 to the next, providing greater assurance that the packages will be properly aligned when stacked. Alternatively, the interlocking features can be formed by removing a portion of the encapsulating material 260, for example, with a laser or a chemical process. In either embodiment, another characteristic of the interlocking features 251 is that they are integrated in the packages 250. As a result, the packages 250 can be stacked without requiring additional jigs or tools, which can be time consuming to position and operate, and can cause damage to the packages 250 if handled improperly.

Figure 5 is a partially schematic, cross-sectional side elevational view of two device packages 350 (shown as an upper package 350a and a lower package 350b) positioned to form a stack 390 in accordance with another embodiment of the invention. In one aspect of this embodiment, each device package 350 can include a support member 330, a microelectronic substrate 320 on the support member 330, and an encapsulating material 360 surrounding the microelectronic substrate 320. In a further aspect of this embodiment, the encapsulating material 360 can be disposed on only an upper surface 336 of the support member 330 and not a lower surface 337. Accordingly, the encapsulating material 360 can

include an upper interlocking feature 351a and the support member 330 can include a corresponding lower interlocking feature 351b (referred to collectively as interlocking features 351).

In one embodiment, the lower interlocking feature 351b can include a cavity or recess in the lower surface 337 of the support member 330. In one aspect of this embodiment, the cavity can be sized and shaped to accommodate a portion of the encapsulating material 360, without altering the encapsulating material 360 from a conventional shape. Accordingly, the upper interlocking feature 351b can be defined by a conventionally-shaped volume of encapsulating material 360. Alternatively, the lower interlocking feature 351b can be sized and shaped to accommodate an upper interlocking feature 351a that has a specialized shape, for example, a protrusion generally similar to that described above with reference to Figure 4. In still further embodiments, the interlocking features 351 can have other shapes and configurations, so long as the interlocking features 351 at least resist relative motion between the packages 350 and provide for alignment of the packages 350.

Figure 6 is a partially schematic, top isometric view of a device package 450 having heat transfer structures 480 in accordance with another embodiment of the invention. In one aspect of this embodiment, the device package 450 includes a microelectronic substrate 420 at least partially enclosed with an encapsulating material 460. In one aspect of this embodiment, a portion of the encapsulating material 460 adjacent to an upper surface 421 of the microelectronic substrate 420 is removed to form a cavity 463 that exposes at least a portion of the upper surface 421. Alternatively, a thin layer 466 of encapsulating material 460 can remain adjacent to the upper surface 421. In either embodiment, the encapsulating material 460 can also be formed into the heat transfer structures 480. For example, the heat transfer structures 480 can include pins 481 that project away from the upper surface 421 of the microelectronic substrate 420, or project away from the thin layer 466 of encapsulating material 460. The thin layer 466 can also transfer heat away from the microelectronic substrate 420, either alone or in conjunction with other heat transfer structures 480. The heat transfer structures 480 can include ribs 482 that project away from the microelectronic substrate 420, or alternatively the heat transfer structures 480 can have other shapes and/or configurations for enhancing the rate at which heat is transferred away from the microelectronic substrate 420. The heat transfer structures 480 can be formed with a laser

process or a chemical or non-chemical process similar to those described above with reference to Figures 2-3. Alternatively, the heat transfer structures 480 can be formed according to other techniques, for example, by molding the heat transfer structures directly into the encapsulating material 460.

One feature of an embodiment of the device package 450 described above with reference to Figure 6 is that the heat transfer structures 480 can be formed directly on the upper surface 421 of the microelectronic substrate 420. Alternatively, the heat transfer structures 480 can be positioned on a thin layer 466 directly adjacent to the upper surface 421. An advantage of either arrangement is that heat can be transferred more directly from the microelectronic substrate 420 to the heat transfer structures 480 and from the heat transfer structures 480 to the surrounding environment than in conventional arrangements that do not include the heat transfer structures 480.

Another feature of an embodiment of the device package 450 described above with reference Figure 6 is that the heat transfer structures 480 can be formed directly in the encapsulating material 460 that surrounds the microelectronic substrate 420. An advantage of this feature is that a separate heat transfer structure (such as a heat sink) need not be separately attached to the microelectronic substrate 420. Accordingly, the thermal connection between the heat transfer structures 480 and the microelectronic substrate 420 can be more secure and thermally transmissive than a connection formed by attaching an initially separate heat sink.

From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but various modifications may be made without deviating from the spirit and scope of the invention. For example, the microelectronic substrates described above with reference to Figures 2-6 can be supported by support members other than PCBs, including lead frames. The bond pads, solder ball pads, solder balls, and wire bonds can be replaced with electrically conductive terminals and connectors having other shapes and configurations. Furthermore, many of the features described above with reference to Figures 2-6 can be combined in accordance with further embodiments of the invention. For example, an embodiment of a microelectronic device package can include heat transfer structures in addition to interlocking features. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A method for packaging a microelectronic substrate, comprising:

disposing an encapsulating material adjacent to a surface of the microelectronic substrate; and

exposing at least a portion of the surface of the microelectronic substrate by removing a portion of the encapsulating material adjacent to the surface of the microelectronic substrate with the microelectronic substrate in an operable condition after the portion of the encapsulating material is removed.

2. The method of claim 1 wherein the microelectronic substrate has a first surface and a second surface facing opposite the first surface, the first surface having a plurality of bond sites for electrical connections to the microelectronic substrate, and further wherein exposing a portion of a surface of the microelectronic substrate includes exposing a portion of the second surface of the microelectronic substrate.

3. The method of claim 1, further comprising:

mounting the microelectronic substrate to a support member with a first surface of the microelectronic substrate facing the support member and a second surface of the microelectronic substrate facing away from the support member;

electrically coupling the microelectronic substrate to the support member;

disposing the encapsulating material adjacent to both the microelectronic substrate and the support member; and

exposing at least a portion of the second surface of the microelectronic substrate by directing laser radiation toward the portion of the encapsulating material adjacent to the second surface to ablate the portion of the encapsulating material.

4. The method of claim 1, further comprising:

selecting the microelectronic substrate to include a memory chip;

mounting the microelectronic substrate to a printed circuit board; and

disposing the encapsulating material adjacent to both the printed circuit board and the microelectronic substrate.

5. The method of claim 1, further comprising transferring heat directly away from the exposed portion of the surface of the microelectronic substrate.

6. The method of claim 1, further comprising convectively transferring heat directly away from the exposed portion of the surface of the microelectronic substrate.

7. The method of claim 1 wherein removing a portion of the encapsulating material includes directing laser radiation toward the encapsulating material.

8. The method of claim 1 wherein removing the portion of the encapsulating material includes directing a laser beam having a power of from about 4 watts to about 25 watts toward the encapsulating material.

9. The method of claim 1 wherein removing the portion of the encapsulating material includes sequentially removing layers of the portion of the encapsulating material by sequentially exposing the layers of encapsulating material to laser radiation.

10. A method for packaging a microelectronic substrate, comprising:

disposing an encapsulating material adjacent to the microelectronic substrate; and

forming a heat transfer structure in an external surface of the encapsulating material by manipulating at least a portion of the encapsulating material to define at least one exposed heat transfer surface of the heat transfer structure.

11. The method of claim 10 wherein manipulating at least a portion of the encapsulating material includes removing a portion of encapsulating material by directing laser radiation toward the encapsulating material.

12. The method of claim 10 wherein the microelectronic substrate has a first surface and a second surface facing opposite the first surface, the first surface having a plurality of bond sites for electrical connections to the microelectronic substrate, and further wherein manipulating at least a portion of the encapsulating material includes removing a portion of the encapsulating material adjacent to the second surface of the microelectronic substrate.

13. The method of claim 10, further comprising:

mounting the microelectronic substrate to a support member;

electrically coupling the microelectronic substrate to the support member;

disposing the encapsulating material adjacent to both the microelectronic substrate and the support member; and

removing at least a portion of the encapsulating material from a region proximate to the microelectronic substrate.

14. The method of claim 10 wherein manipulating the encapsulating material includes removing a portion of the encapsulating material to expose a portion of a surface of the microelectronic substrate initially covered by the encapsulating material.

15. The method of claim 10 wherein forming a heat transfer structure includes forming a cylindrical rod of encapsulating material projecting away from the microelectronic substrate.

16. The method of claim 10 wherein forming a heat transfer structure includes forming a rib projecting away from the microelectronic substrate.

17. A method for packaging a microelectronic substrate, comprising:

positioning at least one of an encapsulating material and a support member adjacent to the microelectronic substrate; and

processing at least one of the encapsulating material and the support member to have an interlocking feature by manipulating a portion of the encapsulating material and/or

the support member, the interlocking feature being configured to engage with a corresponding interlocking feature of another microelectronic substrate package.

18. The method of claim 17 wherein manipulating a portion of the encapsulating material and/or the support member includes directing laser radiation toward the encapsulating material and/or the support member to ablate the portion of the encapsulating material and/or the support member.

19. The method of claim 17 wherein the interlocking feature is positioned in a first surface of the encapsulating material and wherein the method further comprises forming a second interlocking feature in a second surface of the encapsulating material facing opposite the first surface.

20. The method of claim 17 wherein processing the encapsulating material includes forming a recess in the encapsulating material.

21. The method of claim 17 wherein processing the encapsulating material includes forming a projection in the encapsulating material extending away from the microelectronic substrate.

22. The method of claim 17 wherein the microelectronic substrate is electrically coupled to the support member and the interconnecting feature is a first feature formed in the encapsulating material, and wherein the method further comprises processing the support member to form a second interconnecting feature configured to engage the first interconnecting feature of another microelectronic substrate.

23. A method for positioning microelectronic device packages, comprising:

aligning a first microelectronic device package having a first microelectronic substrate and a first encapsulant with a second microelectronic device package having a second microelectronic substrate and a second encapsulant; and

engaging a first interlocking feature of the first microelectronic device package with a second interlocking feature of the second microelectronic device package to at least restrict relative motion between the first and second microelectronic device packages.

24. The method of claim 23, further comprising engaging a tab of the first encapsulant of the first microelectronic device package with a recess in the second encapsulant of the second microelectronic device package.

25. The method of claim 23 wherein the first microelectronic device package includes a support member having a cavity, and wherein the method further comprises receiving the second encapsulant of the second microelectronic device package in the cavity of the support member of the first microelectronic device package.

26. A method for packaging a microelectronic substrate, comprising:

electrically coupling the microelectronic substrate to a support member having a first surface and a second surface facing opposite the first surface, the first surface having a conductive bond pad;

positioning the support member and the microelectronic substrate between two portions of a mold with the first surface and the bond pad of the support member facing a first cavity in the first portion of the mold and the microelectronic substrate facing a second cavity in the second portion of the mold;

disposing an encapsulating material in the first and second cavities of the mold to engage the microelectronic substrate and the bond pad; and

removing a portion of the encapsulating material covering the bond pad to expose the bond pad while the microelectronic substrate remains in an operable condition.

27. The method of claim 26, further comprising:

aligning a first edge of the first cavity with a second edge of the second cavity; and

rigidly supporting the support member in the mold by clamping the support member between the first and second edges.

28. The method of claim 26 wherein removing the portion of the encapsulating material includes directing laser radiation toward the encapsulating material and ablating the portion of the encapsulating material.

29. The method of claim 26 wherein removing the portion of the encapsulating material includes directing a laser beam having a power of from about 4 watts to about 25 watts toward the encapsulating material.

30. The method of claim 26 wherein removing the portion of the encapsulating material includes sequentially removing layers of the portion of the encapsulating material by sequentially exposing the encapsulating material to laser radiation.

31. The method of claim 26, further comprising attaching a solder ball to the bond pad.

32. A method for packaging a microelectronic substrate, comprising:

mounting the microelectronic substrate to a support member with a first surface of the microelectronic substrate facing the support member and a second surface of the microelectronic substrate facing opposite the first surface;

electrically coupling the microelectronic substrate to the support member by passing wire bonds though an aperture in the support member and connecting one end of each wire bond to the support member and an opposite end of each wire bond to the microelectronic substrate;

encapsulating the microelectronic substrate and the support member by disposing an encapsulating material over the support member and the second surface of the microelectronic substrate; and

directing a source of laser radiation toward the second surface of the microelectronic substrate to remove at least a portion of the encapsulating material adjacent to the second surface and expose the second surface.

33. The method of claim 32, further comprising forming a heat transfer feature in the encapsulating material by removing a portion of the encapsulating material to define an exposed external surface of the heat transfer feature.

34. The method of claim 32 wherein directing the source of laser radiation includes directing a laser beam having a power of from about 4 watts to about 25 watts.

35. The method of claim 32 wherein directing the source of laser radiation includes engaging a laser beam with the encapsulating material to remove a first portion of the encapsulating material and engaging the laser beam with the encapsulating material again to remove a second portion of the encapsulating material initially covered by the first portion of the encapsulating material.

36. The method of claim 32 wherein removing a portion of the encapsulating material includes removing a layer of encapsulating material having a thickness of greater than about 0.003 inch.

37. A microelectronic device package formed by a process, comprising:

disposing an encapsulating material adjacent to the microelectronic substrate; and

exposing at least a portion of a surface of the microelectronic substrate by removing a portion of the encapsulating material adjacent to the surface of the microelectronic substrate with the microelectronic substrate in an operable condition after the portion of the encapsulating material is removed.

38. The device package of claim 37 wherein the microelectronic substrate has a first surface and a second surface facing opposite the first surface, the first surface having a plurality of bond sites for electrical connections to the microelectronic substrate, and further wherein exposing a portion of a surface of the microelectronic substrate includes exposing a portion of the second surface of the microelectronic substrate.

39. The device package of claim 37, further comprising removing a portion of the encapsulating material by directing laser radiation toward the portion of the encapasulating material to ablate the portion of the encapsulating material.

40. A microelectronic device package, comprising:

an operable microelectronic die having at least one integrated circuit and a die surface; and

an encapsulating material covering at least a portion of the microelectronic die, the encapsulating material having an external surface and an aperture extending through the external surface to the die surface with a portion of the die surface exposed through the aperture.

41. The package of claim 40, further comprising a support member adjacent to the microelectronic die, and further wherein the microelectronic die is electrically coupled to the support member.

42. The package of claim 40 wherein the microelectronic die has a first surface and a second surface facing opposite the first surface, the first surface having a plurality of terminals for electrical connections to the microelectronic die, the second surface being exposed through the aperture in the encapsulating material.

43. The package of claim 40 wherein the encapsulating material includes heat transfer structures extending transverse to the die surface, the heat transfer structures having exposed, spaced-apart external heat transfer surfaces.

44. The package of claim 40 wherein the encapsulating material includes an interlocking feature positioned to engage a corresponding interlocking feature of another device package to at least resist relative movement between the device packages.

45. A microelectronic device package, comprising:

an operable microelectronic substrate having a first surface and a second surface facing opposite the first surface; and

an encapsulating material and/or a support member covering at least a portion of at least one of the first and second surfaces of the microelectronic substrate, the encapsulating material and/or the support member having an interlocking feature positioned to engage a corresponding interlocking feature of another device package and at least restrict relative movement between the device packages when the interlocking features of the packages are engaged with each other.

46. The device package of claim 45 wherein the microelectronic substrate is at least partially encased in an encapsulating material and the interlocking feature includes a projection in the encapsulating material extending away from the second surface of the microelectronic substrate and positioned to be received in a corresponding recess of the other device package.

47. The device package of claim 45 wherein the interlocking feature includes a recess in the encapsulating material positioned to receive a projection of the other device package.

48. The device package of claim 45, wherein the microelectronic substrate is attached to a support member and the interlocking feature includes a recess in the support member.

49. A pair of microelectronic device packages, comprising:

a first microelectronic device package having a first microelectronic substrate and a first encapsulating material at least partially covering the first microelectronic substrate, the first encapsulating material having an external surface and an aperture in the external surface; and

a second microelectronic device package having a second microelectronic substrate and a second encapsulating material at least partially covering the second

microelectronic substrate, the second encapsulating material having an external surface and a projection extending away from the external surface, the projection being aligned with and received in the aperture of the first encapsulating material when the first microelectronic substrate is adjacent to the second microelectronic substrate.

50. The device packages of claim 49, further comprising a first support member electrically coupled to the first microelectronic substrate and a second support member electrically coupled to the second microelectronic substrate.

51. The device packages of claim 49 wherein at least one of the encapsulating materials includes a heat transfer structure extending transverse to the substrate surface, the heat transfer structures having exposed, spaced-apart external heat transfer surfaces.

52. A microelectronic device package, comprising:

a support member having a conductive link with a first terminal and a second terminal, the second terminal having a bonding surface to form electrical connections with the second terminal;

a microelectronic substrate engaged with the support member and electrically coupled to the first terminal of the conductive link; and

an encapsulating material at least partially covering the microelectronic substrate and the support member, the encapsulating material extending over at least a substantial portion of the bonding surface of the second terminal of the conductive link.

53. The package of claim 52 wherein the support member includes a printed circuit board, the first terminal of the conductive link includes a wire bond pad coupled with a wire bond to the microelectronic substrate, and the second terminal includes a solder ball pad.

54. The package of claim 52 wherein the support member includes a printed circuit board having an aperture, and wherein the package further comprises a wire bond extending through the aperture from the microelectronic substrate to the first terminal.

55. The package of claim 52 wherein the encapsulating material includes an epoxy.

56. A microelectronic device package, comprising:

a microelectronic substrate having a substrate surface; and

an encapsulating material at least partially covering the microelectronic substrate, the encapsulating material defining a plurality of heat transfer structures projecting away from the substrate surface, each heat transfer structure having at least one exposed, external heat transfer surface spaced apart from and facing a heat transfer surface of another of the heat transfer structures.

57. The package of claim 56 wherein the encapsulating material includes an epoxy.

58. The package of claim 56 wherein the heat transfer structures include at least one cylindrical rod of encapsulating material projecting away from the microelectronic substrate.

59. The package of claim 56 wherein the heat transfer structures include at least one rib projecting away from the microelectronic substrate.

60. The package of claim 56 wherein the encapsulating material has an aperture and the surface of the microelectronic substrate is exposed through the aperture in the encapsulating material.

61. A microelectronic device package, comprising:

a microelectronic substrate having a first surface and a second surface facing opposite the first surface;

a support member having a first surface engaged with the first surface of the microelectronic substrate and a second surface facing opposite the first surface, the support

member having an aperture extending therethrough from the first surface to the second surface;

a plurality of bond members extending through the aperture of the support member, the bond members being connected to the microelectronic substrate and the support member; and

an encapsulating material disposed adjacent to the microelectronic substrate and the support member, the encapsulating material having an opening through which a substantial portion of the second surface of the microelectronic substrate is exposed.

62. The package of claim 61 wherein the encapsulating material has at least one heat transfer structure proximate to the second surface of the microelectronic substrate, the heat transfer structure having an exposed external surface positioned to transfer heat from the microelectronic substrate.

63. The package of claim 61 wherein the encapsulating material includes an interlocking feature positioned to engage a corresponding interlocking feature of another package to at least resist relative movement between the packages.

METHOD AND APPARATUS FOR REMOVING ENCAPSULATING MATERIAL FROM A PACKAGED MICROELECTRONIC DEVICE

ABSTRACT

A method and apparatus for encapsulating microelectronic devices. In one embodiment, the method includes removing a portion of encapsulating material that at least partially surrounds a microelectronic substrate by directing a source of laser radiation toward the encapsulating material. The method can further include exposing a surface of the microelectronic substrate, for example, to enhance a rate at which heat is transferred away from the microelectronic substrate. Alternatively, the encapsulating material can be removed to form heat transfer structures, such as pins or ribs, also to enhance a rate at which heat is transferred away from the microelectronic substrate. In still another embodiment, a portion of the encapsulating material or a support member to which the substrate is attached can be removed to define interlocking features that allow one microelectronic substrate package to be stacked on another and to resist relative movement between the two packages.

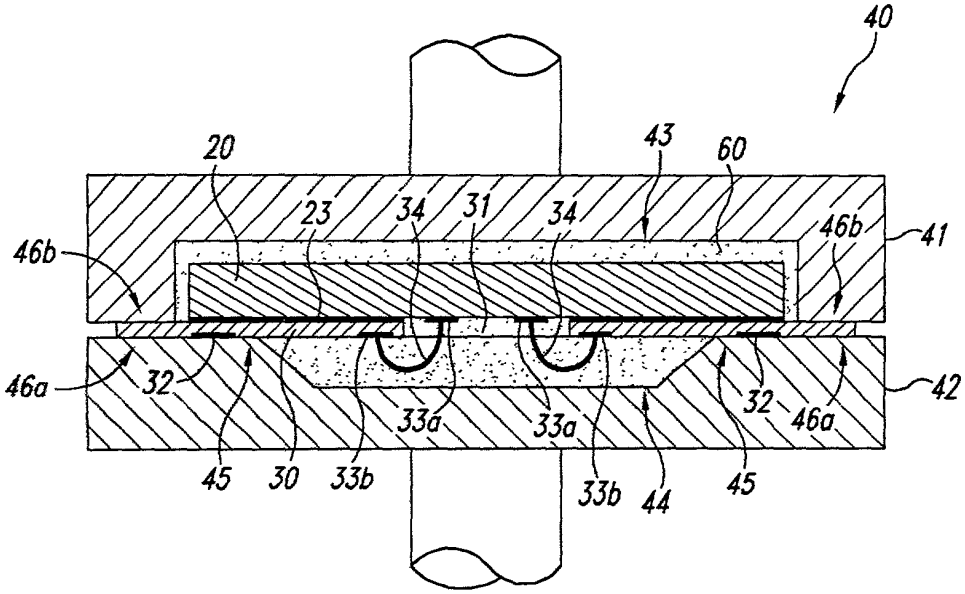

Fig. 1A
(Prior Art)

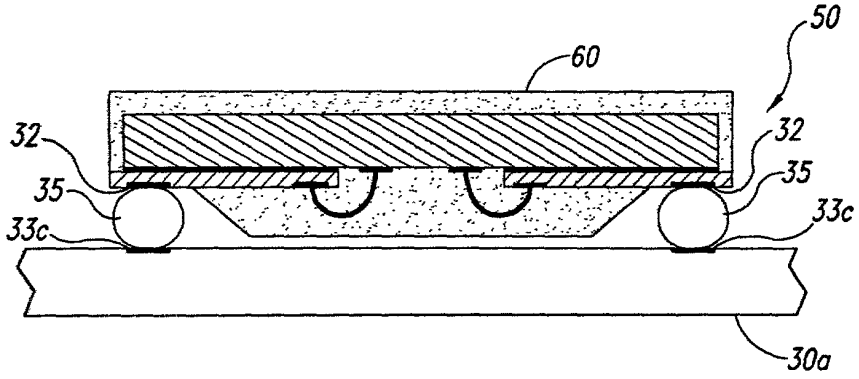

Fig. 1B
(Prior Art)

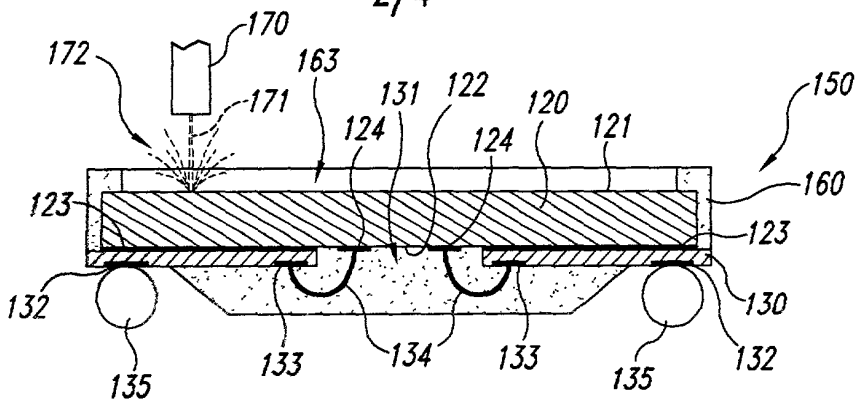

Fig. 2

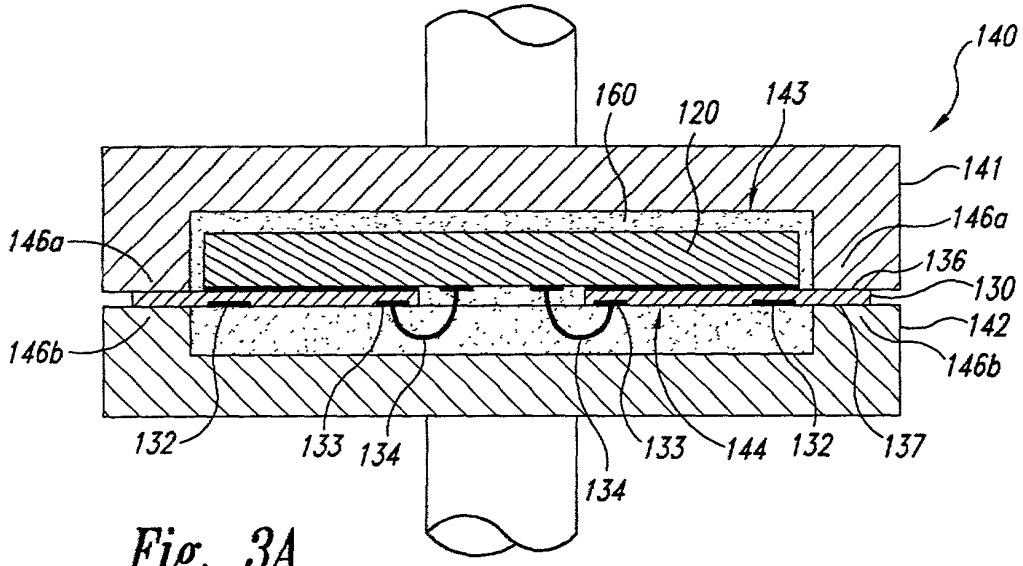

Fig. 3A

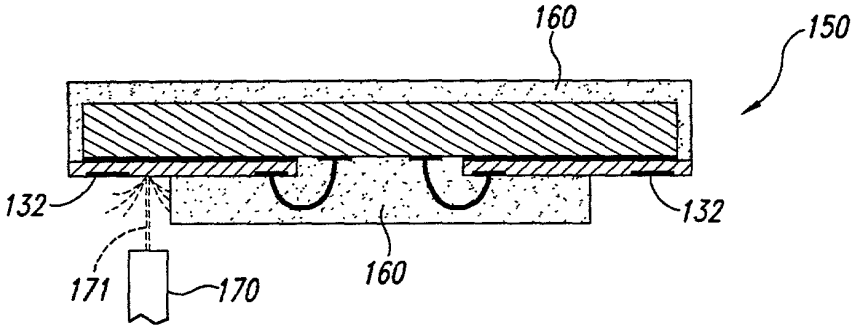

Fig. 3B

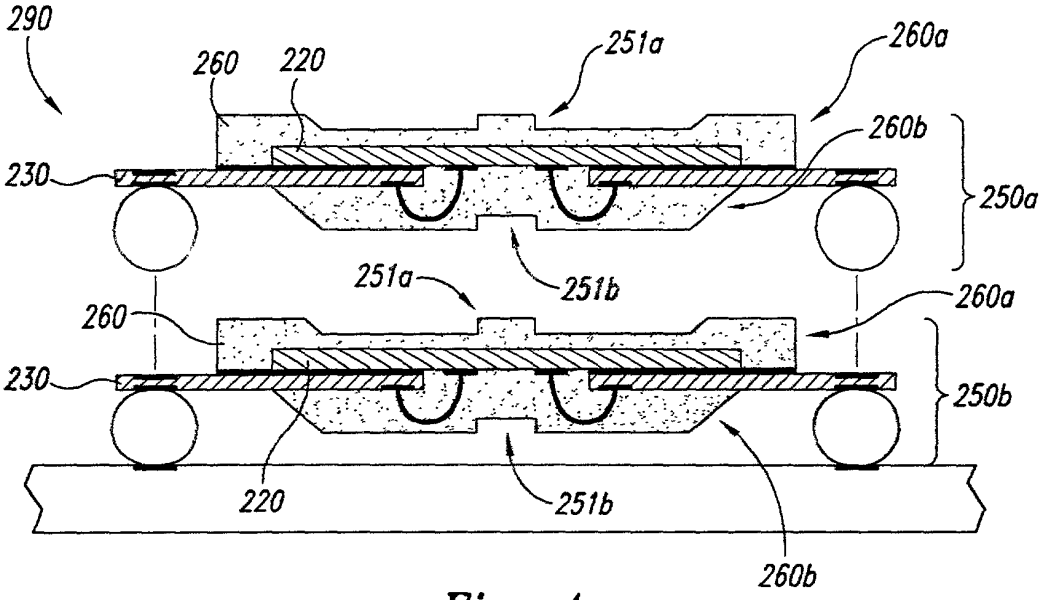
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Fig. 4

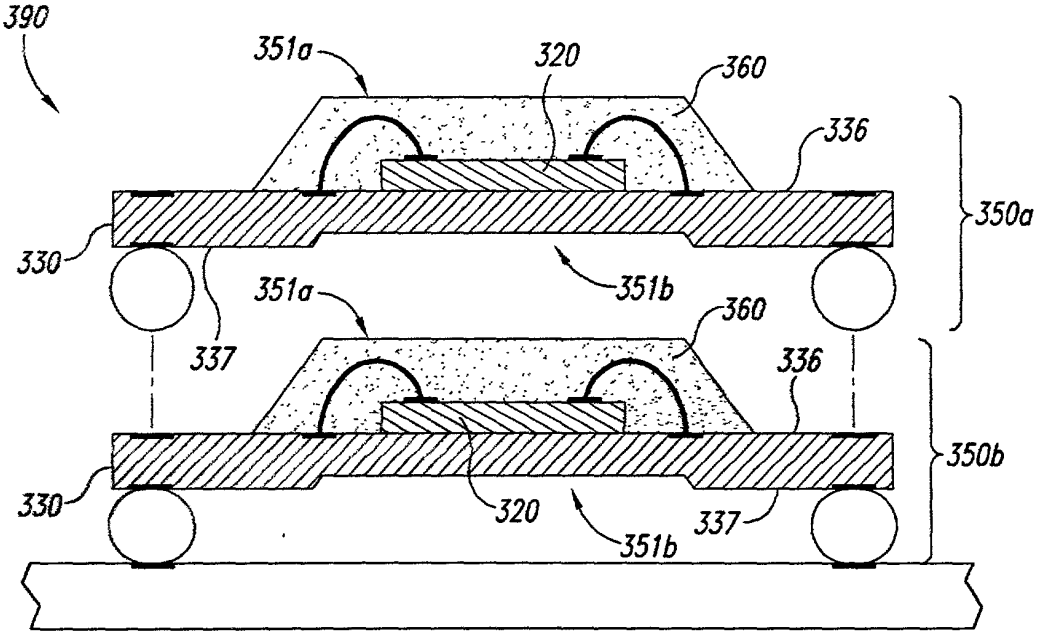
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Fig. 5

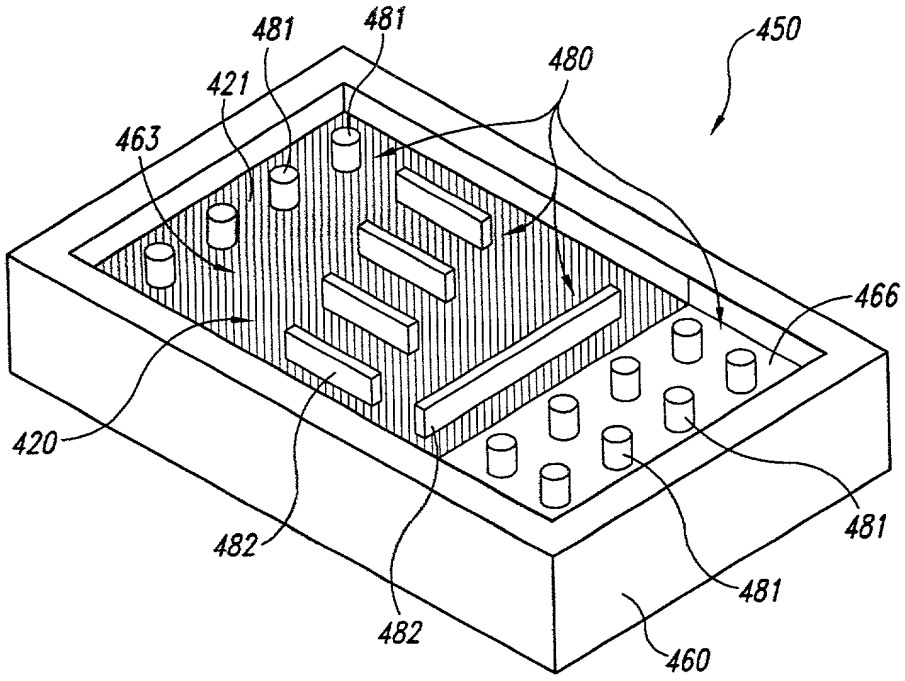

Fig. 6

DECLARATION

As the below-named inventor, I declare that:

My residence, post office address, and citizenship are as stated below under my name.

I believe I am the original, first, and sole inventor of the subject matter claimed and for which a patent is sought on the invention entitled "METHOD AND APPARATUS FOR REMOVING ENCAPSULATING MATERIAL FROM A PACKAGED MICROELECTRONIC DEVICE" in the foregoing specification and claims.

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56(a).

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Joseph M. Brand

Date Aug 11, 2000

Residence : City of Boise
State of Idaho

Citizenship : United States of America

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Boise, ID 83716

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Joseph M. Brand
Filed	:	Concurrently herewith
For	:	METHOD AND APPARATUS FOR REMOVING ENCAPSULATING MATERIAL FROM A PACKAGED MICROELECTRONIC DEVICE
		Docket No. : 108298530US

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment filed concurrently herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor.

Assignee hereby appoints JERRY A. RIEDINGER, Registration No. 30,582; MAURICE J. PIRIO, Registration No. 33,273; JOHN C. STEWART, Registration No. 40,188; MICHAEL D. BROADDUS, Registration No. 41,637; BRIAN P. MCQUILLEN, Registration No. 41,989; TARANEH MAGHAME, Registration No. 43,768; CATHERINE HONG TRAN, Registration No. 43,960; ROBERT G. WOOLSTON, Registration No. 37,263; PAUL T. PARKER, Registration No. 38,264; JOHN M. WECHKIN, Registration No. 42,216; CHRISTOPHER DALEY-WATSON, Registration No. 34,807; STEVEN D. LAWRENZ, Registration No. 37,376; JAMES A.D. WHITE, Registration No.

43,985; FRANK ABRAMONTE, Registration No. 38,066, along with MICHAEL L. LYNCH, Reg. No. 30,871; WALTER D. FIELDS, Reg. No. 37,130; CHARLES B. BRANTLEY, II, Reg. No. 38,086; KEVIN D. MARTIN, Reg. No. 37,882; and DAVID J. PAUL, Reg. No. 34,692, of Micron Technology, Inc., 8000 South Federal Way, Boise, Idaho 83706-9632 as the principal attorneys with full power of substitution, association, and revocation to prosecute said application, to transact all business in the Patent and Trademark Office connected therewith, and to receive the letters patent therefor. Please direct all direct all telephone calls to John M. Wechkin at (206) 583-8888 and telecopies to (206) 583-8500.

Please direct all communications to:

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P. O. Box 1247
Seattle, Washington 98111-1247
Attn: John M. Wechkin

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., filed concurrently herewith for recording, a copy of which is attached hereto, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

MICRON TECHNOLOGY, INC.

8-14-06.
DATE

Michael L. Lynch
Chief Patent Counsel

Enclosure:
Copy of Assignment